CLAIMS

What is claimed is:

1. A rate n/n recursive, systematic convolutional encoder which comprises:

n inputs, wherein n is an integer greater than 1;

n parallel outputs;

an adder having (n+1) inputs and an output; and

a feedback loop, including one or more storage elements in series, coupled to the output of the adder and to an input thereof, the feedback loop and the one or more storage elements being characterized by a prime polynomial;

wherein all n encoder inputs are input to the adder, (n-1) of the encoder inputs are passed through unaltered to form (n-1) of the encoder outputs, and the nth encoder output is derived from the feedback loop.

2. The encoder of claim 1 wherein the feedback loop includes a single storage element having an input and an output, wherein the input of the storage element is coupled to the output of the adder, and the output of the storage element is coupled to an input of the adder, and the nth encoder output is derived from the output of the storage element.

3. The encoder of claim 1 wherein the feedback loop includes a single storage element having an input and an output, and the nth encoder output is derived from the output of the adder, wherein the input of the storage element is coupled to the output of the adder, and the output of the storage element is coupled to an input of the adder.

4. The encoder of claim 1 in which n is 2.

5. The encoder of claim 1 in which n is 3.

6. The encoder of claim 1 in which n is 4.

7. The encoder of claim 1 in which n is 5.

8. The encoder of claim 1 in which n is 6 or greater.

9. The encoder of claim 1 in combination with a D-dimensional bit to symbol mapper, wherein D is an integer greater than or equal to 1.

10. The combination of claim 9 in which the mapper is a Gray mapper.

11. The combination of claim 10 in which the encoder is a rate 3/3 encoder, and the mapper maps each 3-tuple output from the encoder into an 8-PSK symbol.

12. The combination of claim 10 in which the encoder is a rate 6/6 encoder, and the mapper is a four-dimensional mapper which maps each of the two 3-tuples derived from a 6-tuple output from the encoder into an 8-PSK symbol having I and Q (quadrature) components.

13. The combination of claim 10 in which the encoder is a rate 4/4 encoder, and the mapper maps each 4-tuple output from the encoder into a 16-QAM symbol.

14. The combination of claim 10 in which the encoder is a rate 8/8 encoder, and the mapper is a four-dimensional mapper which maps each of the 4-tuples derived from the 8-tuple output from the encoder into a 16-QAM symbol.

15. The combination of claim 10 in which the encoder is a 12/12 encoder, and the mapper is a six-dimensional mapper which maps each of the 4-tuples derived from the 12-tuple output from the encoder into a 16-QAM symbol.

16. The combination of claim 10 in which the encoder is a rate 8/8 encoder, and the mapper maps each 8-tuple output from the encoder into a 256-QAM symbol.

17. The combination of claim 10 in which the encoder is a rate 12/12 encoder, and the mapper is a four-dimensional mapper which maps each of the 6-tuples derived from the 12-tuple output into a 64-QAM symbol.

18. The combination of claim 10 in which the encoder is a rate 12/12 encoder, and the mapper maps each of the 12-tuples output from the encoder into a 4096-QAM symbol.

19. The combination of claim 9 in which D is greater than or equal to 2 and a multiplexor is coupled to the output of the mapper for serializing the D components of each channel symbol.

20. An SCTCM encoder which includes the combination of claim 9 as its inner encoder.

21. An SCTCM encoder which includes the combination of claim 19 as its inner encoder.

22. An SCCC encoder which includes the encoder of claim 1 as its inner encoder.

23. A transmitter which includes the SCTCM encoder of any of claims 20 or 21.

24. A transmitter which includes the SCCC encoder of claim 22.

25. A transceiver which includes the transmitter of any of claims 23 or 24.

26. The transceiver of claim 25 which is a satellite transceiver.

27. The transceiver of claim 25 which is a wireless transceiver.

28. The transceiver of claim 25 which is a wireline transceiver.

29. A wireless device which includes the transceiver of any of claims 26 or 27.

30. The wireless device of claim 29 which is a mobile wireless device.

31. A method of performing TCM modulation comprising the steps of:

providing an n-tuple of bits as an input to the rate n/n encoder of claim 1, wherein n is an integer greater than 1;

receiving an n-tuple of bits as an output from the encoder; and

mapping the n-tuple of output bits into a D-dimensional channel symbol, wherein D is an integer greater than or equal to 1.

32. The method of claim 31 wherein the mapping step employs Gray mapping.

33. The method of claim 31 wherein D=1.

34. The method of claim 31 wherein D>1.

35. The method of claim 34 further comprising serializing the D components of the channel symbol.

36. The combination of claim 10 in which the encoder is a rate 2/2 encoder, and the mapper maps each 2-tuple output from the encoder into two QPSK symbols.

37. The combination of claim 10 in which the encoder is a rate 4/4 encoder, and the mapper maps each of the two 2-tuples derived from the 4-tuple output from the encoder into a QPSK symbol having I and Q components.

38. A method of performing TCM modulation comprising the following steps:

providing a k-tuple of bits as an input to an outer encoder comprising a convolutional encoder having redundancy, the outer encoder producing an n-tuple of bits, where both n and k are integers and n>k;

passing the n-tuple of bits through an interleaver, which outputs an n-tuple of interleaved bits;

providing the n-tuple of interleaved bits as input to an inner encoder comprising the rate n/n encoder of claim 1;

receiving an n-tuple of output bits from the inner encoder; and

mapping the n-tuple of output bits into a D-dimensional channel symbol, where D is an integer greater than or equal to 1.

39. A method of performing SCC modulation comprising the following steps:

providing a k-tuple of bits as an input to an outer encoder comprising a convolutional encoder having redundancy, the outer encoder producing an n-tuple of bits, where both n and k are integers and n>k;

passing the n-tuple of bits through an interleaver, which outputs an n-tuple of interleaved bits;

providing the n-tuple of interleaved bits as input to an inner encoder comprising the rate n/n encoder of claim 1;

receiving an n-tuple of output bits from the inner encoder; and

mapping the n-tuple of output bits into a QPSK or BPSK channel symbol.

40. A method of decoding channel symbols comprising the steps of:

receiving channel symbols as produced by the method of any of claims 38 or 39 after transmission over a channel;

providing the channel symbols through an inner decoder which receives first a prior information and produces first a posteriori information from the channel symbols and the first a priori information;

passing the first a posteriori information through a de-interleaver to produce second a priori information for an outer decoder;

inputting the second a priori information to the outer decoder which produces second a posteriori information;

passing the second a posteriori information from the outer decoder through an interleaver to produce the first a priori information input to the inner decoder;

iterating through the foregoing steps a prescribed number p of iterations, where p is an integer greater than or equal to 1; and

after the prescribed number p of iterations, forming estimates of source bits from third a posteriori information provided by the outer decoder.

41. A SCTCM decoder embodying the method steps of claim 40.

42. A SCCC decoder embodying the method steps of claim 39.

43. A system which comprises a transmitter including the SCTCM encoder of any of claims 20 or 21, and one or more receivers each including the SCTCM decoder of claim 41, the transmitter configured to broadcast information to the one or more receivers over a transmission link.

44. The system of claim 43 wherein the link is a wireless link.

45. The system of claim 43 wherein the link is a wireline link.

46. The system of claim 43 wherein the link is a satellite link.

47. A system which comprises a transmitter including the SCCC encoder of claim 22, and one or more receivers each including the SCCC decoder of claim 42, the transmitter configured to broadcast information to the one or more receivers over a transmission link.

48. The combination of claim 10 in which the encoder is a rate 10/10 encoder, and the mapper is a two-dimensional mapper which maps each 10-tuple output from the encoder into a 1024-QAM channel symbol.

49. The combination of claim 10 in which the encoder is a rate 20/20 encoder, and the mapper is a four-dimensional mapper which maps each of the 10-tuples derived from a 20-tuple output from the encoder into a 1024-QAM channel symbol.

50. The combination of claim 10 in which the encoder is a rate 60/60 encoder, and the mapper is a six-dimensional mapper which maps each of the 10-tuples derived from a 60-tuple output from the encoder into a 1024-QAM symbol.

51. The combination of claim 10 in which the encoder is a rate 9/9 encoder, and the mapper is a six-dimensional mapper which maps each of the three-tuples derived from a 9-tuple output from the encoder into an 8-PSK channel symbol.